EUROPEAN PATENT OFFICE

Patent Abstracts of Japan

PUBLICATION NUMBER : 06291299
PUBLICATION DATE : 18-10-94

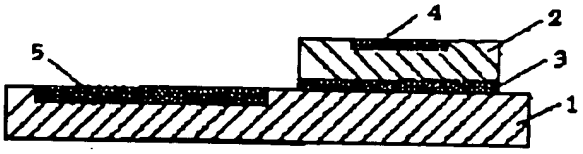
APPLICATION DATE : 28-02-92
APPLICATION NUMBER : 04042879

APPLICANT : MATSUSHITA ELECTRIC IND CO LTD;

INVENTOR : KORIYOU TETSUYOSHI;

INT.CL. : H01L 27/15 H01L 27/14

TITLE : HYBRID INTEGRATED CIRCUIT AND MANUFACTURE THEREOF



ABSTRACT : PURPOSE: To produce a low-cost optical hybrid integrated circuit of large scale integration with high yield by providing an InP substrate coated selectively with silicon or its oxide where the InP substrate and a silicon substrate are joined.

CONSTITUTION: Electronic devices 5 such as transistors are formed on an Si substrate 1. Optical devices 4 such as a laser are formed on a InP substrate 2 including a silicon oxide film 3, which comes into direct contact with the silicon substrate. The electronic devices and optical devices on the two substrates are functionally connected through electrical interconnections to form large scale integration. Since the Si substrate 1 has a large thermal conductivity, heat dissipation is adequate if a high-power laser is formed on the InP substrate 2.

(19) Japanese Patent Office (JP)

(12) Unexamined Patent Gazette (A)

(11) Unexamined Patent Application

No. 6-291299

(43) Published October 18, 1994

---

(51) Int. Cl.[5]	ID Symbol	Internal File No.	FI	Tech. Indic.
H01L 27/15		8934-4M		
27/14				
		7210-4M	HI01L, 27/14	J

Request for Examination: submitted
Number of Claims: 12 OL (6 pages total)

---

(21) Application No.: 4-42879
(22) Application Date: February 28, 1992

(71) Applicant: 00005821
Matsushita Electric Industrial Co., Ltd.
1006 Oaza Kadoma

(72) Inventor: Kazuo Eda
c/o Matsushita Electric Industrial Co., Ltd.
1006 Oaza Kadoma
Kadoma-shi, Osaka Prefecture

(72) Inventor: Yutaka Taguchi
c/o Matsushita Electric Industrial Co., Ltd.
1006 Oaza Kadoma
Kadoma-shi, Osaka Prefecture

(72) Inventor: Akio Kanehoshi
c/o Matsushita Electric Industrial Co., Ltd.
1006 Oaza Kadoma
Kadoma-shi, Osaka Prefecture

(74) Representative: Masamichi Matsuda, Patent Attorney

continued on last page

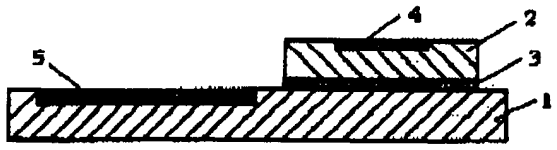
---

(54) Title of the Invention: Hybrid Integrated Circuit and Manufacture Thereof

(57) [Abstract]

[Purpose] To offer a hybrid integrated circuit and manufacture thereof that can integrate optical elements and electronic elements at high density, has good yield at low cost, and obtains satisfactory characteristics.

[Constitution] A hybrid integrated circuit that has InP substrate 2, and Si substrate 1 bonded to InP substrate 2 by silicon oxide film or silicon film 3 formed at a particular site on this InP substrate 2.



1 Si substrate
2 InP substrate
3 silicon oxide film or silicon film
4, 4' optical element
5 electronic element

[Claims]

[Claim 1] Hybrid integrated circuit so characterized that it has an InP substrate, and an Si substrate bonded to this InP substrate by a silicon oxide film or silicon film formed at a particular site on the above-mentioned InP substrate.

[Claim 2] Hybrid integrated circuit described in Claim 1 so characterized that the silicon film is an amorphous silicon film.

[Claim 3] Hybrid integrated circuit described in Claim 1 so characterized that the silicon film is a polycrystalline silicon film.

[Claim 4] Hybrid integrated circuit described in Claim 1, 2, or 3 so characterized that optical elements such as at least a semiconductor laser are formed on the InP substrate, and electronic elements such as at least a transistor are formed on the above-mentioned Si substrate.

[Claim 5] Hybrid integrated circuit described in Claim 4 so characterized that a light emitting element is formed on one surface and a light receiving element is formed on the other surface at particular sites on the opposing bonded surfaces of the above-mentioned InP substrate and the above-mentioned Si substrate such that light emitted from the above-mentioned light emitting element is incident on the above-mentioned light receiving element.

[Claim 6] Manufacture of hybrid integrated circuit so characterized that after subjecting each of an Si substrate and an InP substrate to a semiconductor process treatment to be performed at or above a particular temperature to reinforce bonding, a silicon oxide film or silicon film is formed on all or part of the surface of the above-mentioned InP substrate, the surface of the silicon oxide film or silicon film formed on the above-mentioned InP substrate is bonded to a particular site on the above-mentioned Si substrate, and after performing a semiconductor process treatment at or above the above-mentioned particular temperature to reinforce the bonding strength of this site, from the above-mentioned particular temperature or lower, a circuit is integrated on the above-mentioned InP substrate and the above-mentioned Si substrate by performing a semiconductor process treatment to be performed at a temperature lower than the above-mentioned particular temperature.

[Claim 7] Manufacture of hybrid integrated circuit described in Claim 6 so characterized that the Si substrate is bonded to the above-mentioned silicon oxide film or silicon film by way of hydroxyl groups.

[Claim 8] Manufacture of hybrid integrated circuit described in Claim 7 so characterized that the InP substrate and the Si substrate are bonded by applying a particular voltage to the above-mentioned silicon oxide film or silicon film in between while the InP substrate and the Si substrate are heated.

[Claim 9] Manufacture of hybrid integrated circuit described in Claim 8 so characterized that the above-mentioned particular temperature to reinforce the bonding strength of the above-mentioned bonding site is a temperature in a range from 100°C to 700°C.

[Claim 10] Manufacture of hybrid integrated circuit described in Claim 9 so characterized that the above-mentioned silicon film formed on the InP substrate is an amorphous silicon film.

[Claim 11] Manufacture of hybrid integrated circuit described in Claim 9 so characterized that the above-mentioned silicon film formed on the InP substrate is a polycrystalline silicon film.

[Claim 12] Manufacture of hybrid integrated circuit so characterized that after subjecting each of an Si substrate and an InP substrate to a semiconductor process treatment to be performed at or above a particular temperature to reinforce bonding, a silicon oxide film or silicon film is formed on all or part of the surface of the above-mentioned InP substrate, a silicon oxide film or silicon film is formed on all or part of the surface of the above-mentioned Si substrate, the surface of the silicon oxide film or silicon film formed on the above-mentioned InP substrate is bonded to the surface of the silicon oxide film or silicon film formed on the above-mentioned Si substrate, and after performing a semiconductor process treatment at or above the above-mentioned particular temperature to reinforce the bonding strength of this bonding site, from the above-mentioned particular temperature or lower, a circuit is integrated on the above-mentioned InP substrate and the above-mentioned Si substrate by performing a semiconductor process treatment to be performed at a temperature lower than the above-mentioned particular temperature.

[Detailed Explanation of the Invention]

[0001]

[Industrial Field of Application]

This invention pertains to a high-performance hybrid integrated circuit that uses InP and Si, and manufacture thereof.

[0002]

[Prior Art]

For hybrid integrated circuits such as, for example, optical-electronic integrated circuits that integrate a semiconductor laser and a drive transistor or amplifying transistor, a method is known in prior art in which an optical element such as a semiconductor laser and an electronic element such as a transistor are produced simultaneously on a substrate such as InP on which a semiconductor laser can be fabricated.

[0003]

[Problems that the Invention is to Solve]

The method described above that integrates both an optical element and an electronic element on an InP substrate has, however, problems such as because an InP substrate is several times more expensive than an Si substrate and the semiconductor device formation process is more complicated than on an Si substrate, yield is poor and the circuit cannot be integrated at high density. In addition, this method has problems such as because an InP substrate has several times worse heat conductivity than an Si substrate, it is not suitable for integrating circuits that use a large amount of electric power.

[0004]

Reflecting on such problems in the prior art, the purpose of this invention is to offer a hybrid integrated circuit and manufacture thereof that can integrate optical elements and electronic elements at high density, has good yield at low cost, and obtains satisfactory characteristics.

[0005]

[Means of Solving the Problems]

The invention of Claim 1 is a hybrid integrated circuit that has an InP substrate, and an Si substrate bonded to this InP substrate by a silicon oxide film or silicon film formed at a particular site on the InP substrate.

[0006]

The invention of Claim 6 is the manufacture of a hybrid integrated circuit in which, after subjecting both an Si substrate and an InP substrate to a semiconductor process treatment to be performed at or above a particular temperature to reinforce bonding, a silicon oxide film or silicon film is formed on all or part of the surface of the InP substrate, the surface of the silicon oxide film or the silicon film formed on the InP substrate is bonded to a particular site on the Si substrate, and after performing a semiconductor process treatment at or above the particular temperature to reinforce the bonding strength of this site, from this particular temperature or lower, a circuit is integrated on the InP substrate and the Si substrate by performing a semiconductor process treatment to be performed at a temperature lower than the particular temperature.

[0007]

[Operation]

In the invention of Claim 1, a silicon oxide film or silicon film formed on an InP substrate is bonded to an Si substrate to form an integrated circuit that combines an InP substrate and an Si substrate.

[0008]

In the invention of Claim 6, because the surface of a silicon oxide film or silicon film formed on an InP substrate is bonded to a particular site on an Si substrate and heat treatment is performed at a particular temperature to reinforce the bonding strength of this site, an InP substrate and an Si substrate can be bonded easily with adequate bonding strength.

[0009]

[Embodiments]

Embodiments of the hybrid integrated circuit and manufacture thereof with which this invention is concerned are explained below while referring to the figures.

[0010]

Embodiment 1

Figure 1 is a schematic cross-section that shows the structure of the hybrid integrated circuit of the first embodiment of this invention. That is, electronic element 5 such as a transistor is formed on Si substrate 1 on which a hybrid integrated circuit is constituted, and optical element 4 such as a semiconductor laser is formed on InP substrate 2. In addition, silicon oxide film (or silicon film) 3 is formed on a particular surface of InP substrate 2, and this silicon oxide film (or silicon film) 3 and Si substrate 1 are bonded directly (the bonding method is explained later). Optical element 4 and electronic element 5 formed on each of these substrates are connected functionally by a means such as an electrical circuit pattern.

[0011]

As explained above, optical element 4 is formed on InP substrate 2 that has superior optical characteristics such as light emission, and electronic element 5 such as a transistor is formed on Si substrate 1 that is applied when forming a large-scale integrated circuit. As a result, a high-performance optical element 4 and a large-scale integrated electronic element 5 can be integrated together. In addition, because Si substrate 1 has high heat conductivity, it can radiate heat adequately even when a high-output semiconductor laser is formed on InP substrate 2. Therefore, electronic elements such as power amplifiers can also be integrated on this substrate.

[0012]

Embodiment 2

Figure 2 is a schematic section that shows the structure of the hybrid integrated circuit of the second embodiment of this invention. That is, electronic element 5 such as a transistor is formed on Si substrate 1 on which a hybrid integrated circuit is constituted, and optical element (light emitting element) 4 such as a semiconductor laser is formed on part of the surface of InP substrate 2 that faces Si substrate 1. In addition, silicon oxide film (or silicon film) 3 is formed on a particular site on this surface around optical element (light emitting element) 4, and this silicon oxide film (or silicon film) 3 and Si

substrate 1 are bonded directly (the bonding method is explained later). Furthermore, optical element (light receiving element) 4' such as a photodiode is formed on a site on Si substrate 1 that faces optical element (light emitting element) 4 formed on InP substrate 2, and these optical element (light emitting element) 4 and optical element (light receiving element) 4' are placed such that they are optically coupled. As required, optical elements 4 and 4' and electronic element 5 formed on each of these substrates are connected functionally by a means such as an electrical circuit pattern.

[0013]

As explained above, optical element 4 such as a semiconductor laser is formed on InP substrate 2 that has superior optical characteristics such as light emission, and a partial optical element 4' such as a photodiode that obtains high performance even on Si substrate 1 and electronic element 5 such as a transistor are formed on Si substrate 1 that is applied when forming a large-scale integrated circuit. As a result, high-performance optical elements 4 and 4' and a large-scale integrated electronic element 5 can be integrated together. As a result, the same effects are obtained as in Embodiment 1. In addition, in this case, the large-scale integrated circuit on Si substrate 1 and optical element 4 on InP substrate 2 described above can transmit signals directly by light without relying on an electrical circuit pattern. In addition, high-speed electronic elements can be integrated on InP substrate 2 simultaneously.

[0014]

Moreover, in both of the embodiments described above, an amorphous silicon film or a polycrystalline silicon film may be used instead of the silicon oxide film formed on the InP substrate.

[0015]

In addition, in the embodiment described above, the two substrates were coupled optically by forming a light emitting element on the InP substrate side and a light receiving element on the Si substrate side, but the two substrates also may be coupled optically by forming a light emitting element on the Si substrate side and forming a light receiving element on the InP substrate side.

[0016]

In addition, in the embodiment described above, space was left between the light emitting element and the light receiving element, but regardless of this, this need only be constructed such that light emitted from the light emitting element is incident on the light receiving element.

[0017]

Embodiment 3

Manufacture of a hybrid integrated circuit that is the third embodiment of this invention is explained.

[0018]

First, a particular place on an Si substrate and an InP substrate was subjected to a series of semiconductor process treatments that includes processes such as a diffusion process to be performed at or above the heat treatment temperature required to reinforce bonding strength, and an electronic element such as a field effect transistor (FET) and an optical element such as a semiconductor laser were formed. Normally, these processes such as a diffusion process are performed at a high temperature of 1000°C or greater.

[0019]

Next, after forming a protective film on the Si part and the InP part where each type of element was formed, other exposed Si surface parts and InP surface parts were cleaned carefully. Specifically, the surface layer of the InP substrate was etched by an ammonia etching solution and removed by hydrogen peroxide. Similarly, the surface of the Si substrate was cleaned by a hydrofluoric acid etching solution. During this, the protective film was removed only from required parts. Following this, a silicon oxide film was formed on the InP substrate by a method such as chemical vapor deposition. The thickness of the film was about 0.1 to 3 micrometers. This thickness and uniformity at this thickness are easy to control. Furthermore, the surface of the silicon oxide film was cleaned by buffered hydrofluoric acid. During this, the protective film was removed only from required parts.

[0020]

Next, when the surface of the silicon oxide film was cleaned well with purified water and the exposed parts of the above-mentioned Si substrate were layered evenly over the silicon oxide film on the above-mentioned InP substrate, a direct bond was obtained by hydroxyl groups adsorbed to the surface of the silicon oxide film and the surface of the Si substrate. Although adequate bonding strength was obtained without further treatment, this bond was further reinforced when heat treatment was performed at a temperature from 100°C to 700°C. Increasing the temperature of this heat treatment imposes some restrictions on shape and dimensions due to the difference between the coefficient of thermal expansion of the InP substrate and the coefficient of thermal expansion of the Si substrate, but basically, the higher the temperature of heat treatment, the more bonding strength can be improved without the bonded substrates peeling or breaking when they are made thinner and smaller in area.

[0021]

Next, this was subjected to various types of processes such as electrode formation to be performed at or below the temperature of heat treatment to reinforce bonding strength, and a circuit pattern was formed. A material such as aluminum or gold was used for the circuit. As a result, a hybrid integrated circuit with the structure shown in Embodiment 2 was obtained. As a result of heat treatment to reinforce bonding, just by keeping for one hour at 200°C, for example, bonding strength was increased several times and a bonding strength of several tens of kg/cm^2 was obtained. When the temperature was raised to 700°C or higher, surface characteristics greatly deteriorated due to P (phosphorus) being drawn from the surface of the InP substrate, and optical elements did not achieve the desired performance. As a result, the temperature of bonding heat treatment is preferably 700°C or lower.

[0022]

Using a general adhesive such as resin to bond between Si substrate 1 and silicon oxide film (or silicon film) 3 has problems such as semiconductor processes cannot be performed after bonding in terms of surface heat resistance and shock resistance. When the method of this embodiment is used, however, the Si substrate and the InP substrate are bonded directly, and such problems are solved.

[0023]

In addition, when adhering using an adhesive such as resin, because it is difficult to control the thickness of the adhesive with high precision, substrates have a poor degree of parallel after adhering and photolithography precision is poor, but this invention solves these problems. In addition, because bonding directly improves heat conductivity, it can be applied to circuits that have high energy consumption.

[0024]

It is considered that the mechanism of the direct bonding described above is that by immersing the surface of the silicon film or silicon oxide film in purified water after performing an appropriate surface treatment, hydroxyl groups adhere to this surface and bonding is performed by the hydroxyl groups adhering to both surfaces. It is considered that when heat treatment is performed following this, bonding is reinforced by mutual diffusion.

[0025]

Embodiment 4

Manufacture of a hybrid integrated circuit that is the fourth embodiment of this invention is explained.

[0026]

An electronic element or optical element was formed on a particular place on an Si substrate and an InP substrate in the same way as in Embodiment 3. Next, after forming a protective film and cleaning the surface, an amorphous silicon film was formed on the InP substrate that became the bonding surface by a means such as plasma CVD. The thickness of the amorphous silicon film formed was roughly the same as in Embodiment 3, or about 0.1 to 3 micrometers. Next, the surfaces of the amorphous silicon film and the Si substrate were cleaned carefully in the same way as in Embodiment 3. The concrete method was roughly the same as in Embodiment 3. The surface of the amorphous silicon film was cleaned by a buffered hydrofluoric acid etching solution. Next, by cleaning the surfaces of the amorphous silicon film and the Si substrate carefully with purified water, then immediately layering

these evenly, bonding was obtained easily by hydroxyl groups adsorbed to the surface of the amorphous silicon film.

[0027]

Next, by performing processes in the same way as in Embodiment 3 as required, a hybrid integrated circuit could be manufactured that had an optical element formed on an InP substrate integrated together with an electronic element formed on an Si substrate, and comparable effects to Embodiment 3 were obtained. The bonding strength obtained in this case was two to five times that obtained using silicon oxide film.

[0028]

Embodiment 5

Manufacture of a hybrid integrated circuit that is the fifth embodiment of this invention is explained.

[0029]

An electronic element or optical element was formed on a particular place on an Si substrate and an InP substrate in the same way as in Embodiment 3 or 4. Next, after forming a protective film and cleaning the surface, a silicon oxide film or amorphous silicon film was formed on the InP substrate that became the bonding surface. Next, the surfaces of the silicon oxide film or amorphous silicon film and the Si substrate were cleaned carefully in the same way as in Embodiment 3 or 4. The concrete method was roughly the same as in Embodiment 3 or 4. The surface of the silicon oxide film or amorphous silicon film was cleaned by a buffered hydrofluoric acid etching solution. Next, the surface of the silicon oxide film or amorphous silicon film was cleaned well with purified water, and the surfaces to be bonded were layered.

[0030]

After drying, a high-voltage direct current was applied to the silicon oxide film or amorphous silicon film part while heating both substrates. As a result, a firm direct bond was obtained by the action of electrostatic force. Next, by performing processes in the same way as in Embodiment 3 as required, a

hybrid integrated circuit could be manufactured that had an optical element formed on an InP substrate integrated together with an electronic element formed on an Si substrate, and comparable effects to Embodiment 3 were obtained. Bonding strength in this case was still stronger than when treated only by heat treatment

[0031]

During this, high voltage can be applied more effectively to the silicon oxide film or amorphous silicon film used for bonding by using a semiconductor substrate for the Si substrate and the InP substrate or by installing a high resistance part on part of the substrates such that a high voltage can be applied to film on the bonded part. In this case, silicon oxide film is intrinsically a high conductor, but amorphous silicon film preferably should have as high resistance as possible.

[0032]

For the voltage applied, from 50 to 1000 V per one micrometer film thickness is appropriate. When voltage is high, it is better to apply the voltage in pulses.

[0033]

Embodiment 6

Manufacture of a hybrid integrated circuit that is the sixth embodiment of this invention is explained.

[0034]

An electronic element or optical element was formed on a particular place on an Si substrate and an InP substrate in the same way as in Embodiment 3. Next, after forming a protective film and cleaning the surface, a polycrystalline silicon film was formed on the InP substrate that became the bonding surface by a means such as plasma CVD. The thickness of the amorphous silicon film formed was roughly the same as in Embodiment 3, or about 0.1 to 3 micrometers. Next, the surfaces of the polycrystalline silicon film and the Si substrate were cleaned carefully in the same way as in Embodiment 3. The concrete method was roughly the same as in Embodiment 3. The surface of the polycrystalline silicon film was cleaned by a buffered hydrofluoric acid etching solution. Next, by

cleaning the surfaces of the polycrystalline silicon film and the Si substrate well with purified water, then immediately layering these evenly, bonding was obtained easily by hydroxyl groups adsorbed to the surface of the polycrystalline silicon film. Next, by performing processes in the same way as in Embodiment 3 as required, a hybrid integrated circuit could be manufactured that had an optical element formed on an InP substrate integrated together with an electronic element formed on an Si substrate, and comparable effects to Embodiment 3 were obtained.

[0035]

Moreover, all of the embodiments of manufacture of a hybrid integrated circuit described above were explained for the example of the structure of Embodiment 2, but the structure of Embodiment 1 can be achieved simply by forming the silicon oxide film or silicon film on the back of the InP substrate in each of the embodiments of manufacture. In this case, wiring between the optical element or the like on the InP substrate and the electronic element or the like on the Si substrate can be accomplished by a means such as wiring externally or forming via holes in the InP substrate.

[0036]

In addition, in all of the embodiments described above, no other film was formed on the Si substrate, but direct bonding can be achieved in the same way even when a silicon oxide film or silicon film is also formed on the Si substrate.

[0037]

In addition, in all of the embodiments described above, the flatness of the film surface used for bonding is important. Because poor film formation method or conditions or large surface irregularities make bonding difficult, adequate care is required.

[0038]

In addition, in all of the embodiments described above, because an electronic element or the like formed on an Si substrate and an optical element or the like formed on an InP substrate first then are integrated together, a hybrid integrated circuit can be made that is greatly miniaturized and light in weight.

[0039]

In addition, because a large-scale integrated circuit can be formed on an Si substrate that can be formed with good yield and optical elements can be formed on an InP substrate that obtains high performance, a hybrid integrated circuit is obtained that has higher performance and better yield than circuits integrated using a single substrate.

[0040]

In addition, in all of the embodiments, because the bonding method was direct bonding of an InP substrate and an Si substrate by an inorganic silicon material controlled for film thickness, flatness is extremely good, the photolithography on the sub-micrometer scale required for large-scale integration can be performed, and reliability against heat and vibration also is greatly improved.

[0041]

[Effects of the Invention]

As should be clear from the explanation above, this invention has the advantages that it can integrate optical elements and electronic elements at high density, has good yield at low cost, and obtains satisfactory characteristics.

[Brief Explanation of the Figures]

Figure 1 is a schematic section that shows the structure of the hybrid integrated circuit of the first embodiment of this invention.

Figure 2 is a schematic section that shows the structure of the hybrid integrated circuit of the second embodiment of this invention.

[Key to Part Numbers]

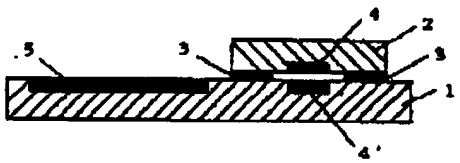
1 Si substrate
2 InP substrate
3 silicon oxide film or silicon film
4 optical element (light emitting element)
4' optical element (light receiving element)
5 electronic element

FIG. 1

【図1】

FIG. 2

【図2】



1 Si substrate
2 InP substrate
3 silicon oxide film or silicon film
4, 4' optical element
5 electronic element

continued from the front page:

(72) Inventor: Tetsuyoshi Ogura
c/o Matsushita Electric Industrial Co., Ltd.
1006 Oaza Kadoma
Kadoma-shi, Osaka Prefecture

(19)日本国特許庁（ＪＰ）　(12) **公開特許公報（A）**　(11)特許出願公開番号

特開平6－291299

(43)公開日　平成６年(1994)10月18日

(51)Int.Cl.[5]	識別記号	庁内整理番号	ＦＩ		技術表示箇所
Ｈ０１Ｌ　27/15		8934－4M			
27/14					
		7210－4M	Ｈ０１Ｌ　27/ 14	Ｊ	

審査請求　有　　請求項の数12　ＯＬ　（全 6 頁）

(21)出願番号　特願平4－42879

(22)出願日　平成４年(1992)２月28日

(71)出願人　000005821
松下電器産業株式会社
大阪府門真市大字門真1006番地

(72)発明者　江田　和生
大阪府門真市大字門真1006番地　松下電器産業株式会社内

(72)発明者　田口　豊
大阪府門真市大字門真1006番地　松下電器産業株式会社内

(72)発明者　金星　章大
大阪府門真市大字門真1006番地　松下電器産業株式会社内

(74)代理人　弁理士　松田　正道

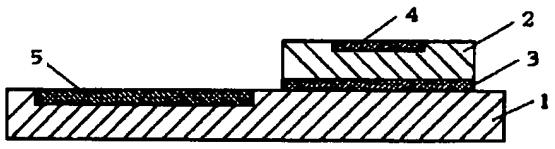
最終頁に続く

(54)【発明の名称】　ハイブリッド集積回路とその製造方法

(57)【要約】

【目的】　光素子及び電子素子を高密度に集積化でき、低コストで歩留まりがよく、良好な特性が得られるハイブリッド集積回路とその製造方法を提供すること。

【構成】　ＩｎＰ基板２と、そのＩｎＰ基板２の所定の部位に形成された酸化珪素膜または珪素膜３によって、ＩｎＰ基板２に接合されているＳｉ基板１とを備える。



1　Ｓｉ基板
2　ＩｎＰ基板
3　酸化珪素膜または珪素膜
4、4'　光素子
5　電子素子

1

【特許請求の範囲】

【請求項1】　ＩｎＰ基板と、そのＩｎＰ基板の所定の部位に形成された酸化珪素膜または珪素膜によって、前記ＩｎＰ基板に接合されているＳｉ基板とを備えたことを特徴とするハイブリッド集積回路。

【請求項2】　珪素膜は、非晶質の珪素膜であることを特徴とする請求項1記載のハイブリッド集積回路。

【請求項3】　珪素膜は、多結晶の珪素膜であることを特徴とする請求項1記載のハイブリッド集積回路。

【請求項4】　ＩｎＰ基板上には、少なくとも半導体レーザなどの光素子が形成され、前記Ｓｉ基板上には、少なくともトランジスタなどの電子素子が形成されていることを特徴とする請求項1、2又は3記載のハイブリッド集積回路。

【請求項5】　接合された前記ＩｎＰ基板及び前記Ｓｉ基板の対向面の所定の部位に、一方に発光素子が形成され、他方に受光素子が形成され、前記発光素子から出射される光が前記受光素子に入射されるようになっていることを特徴とする請求項4記載のハイブリッド集積回路。

【請求項6】　Ｓｉ基板およびＩｎＰ基板のそれぞれに、接合強化のための所定温度以上の温度で処理すべき半導体プロセス処理を行った後、前記ＩｎＰ基板の全面又は一部に、酸化珪素膜または珪素膜を形成し、前記ＩｎＰ基板上に形成された前記酸化珪素膜または珪素膜の面を、前記Ｓｉ基板の所定部位に接合させ、その部位の接合力を強化するために前記所定温度で熱処理を行った後、前記所定温度以下の温度により、前記ＩｎＰ基板及び前記Ｓｉ基板上に、前記所定温度を下回る温度で処理すべき半導体プロセス処理を行うことによって集積化したことを特徴とするハイブリッド集積回路の製造方法。

【請求項7】　Ｓｉ基板と前記酸化珪素膜または珪素膜との接合は、水酸基を介してなされることを特徴とする請求項6記載のハイブリッド集積回路の製造方法。

【請求項8】　ＩｎＰ基板及びＳｉ基板を加熱しながら、前記酸化珪素膜または珪素膜間に所定の電圧をかけることによって、ＩｎＰ基板とＳｉ基板を接合することを特徴とする請求項7記載のハイブリッド集積回路の製造方法。

【請求項9】　接合部位の前記接合力を強化するための前記所定温度は、１００度Ｃから７００度Ｃの温度範囲であることを特徴とする請求項8記載のハイブリッド集積回路の製造方法。

【請求項１０】ＩｎＰ基板上に形成した前記珪素膜は、非晶質の珪素膜であることを特徴とする請求項9記載のハイブリッド集積回路の製造方法。

【請求項１１】ＩｎＰ基板上に形成した前記珪素膜は、多結晶の珪素膜であることを特徴とする請求項9記載のハイブリッド集積回路の製造方法。

【請求項１２】　Ｓｉ基板およびＩｎＰ基板のそれぞれに、接合強化のための所定温度以上の温度で処理すべき半導体プロセス処理を行った後、前記ＩｎＰ基板の全面又は一部に、酸化珪素膜または珪素膜を形成し、前記Ｓｉ基板の全面又は一部に、酸化珪素膜又は珪素膜を形成し、前記ＩｎＰ基板上に形成された前記酸化珪素膜または珪素膜の面を、前記Ｓｉ基板に形成された前記酸化珪素膜又は珪素膜の面に接合させ、その接合部位の接合力を強化するために前記所定温度で熱処理を行った後、前記所定温度以下の温度により、前記ＩｎＰ基板及び前記Ｓｉ基板上に、前記所定温度を下回る温度で処理すべき半導体プロセス処理を行うことによって集積化することを特徴とするハイブリッド集積回路の製造方法。

2

【発明の詳細な説明】

【０００１】

【産業上の利用分野】本発明は、ＩｎＰとＳｉを用いた高性能なハイブリッド集積回路及びその製造方法に関するものである。

【０００２】

【従来の技術】従来、ハイブリッド集積回路、例えば半導体レーザーと駆動トランジスタや増幅用トランジスタなどを集積化した光電子集積回路などでは、ＩｎＰなどの半導体レーザー作製可能な基板の上に、半導体レーザーなどの光素子とトランジスタなどの電子素子を同時に作り込む方法が知られている。

【０００３】

【発明が解決しようとする課題】しかしながら、上記のＩｎＰ基板に光素子と電子素子の両者を集積する方法では、ＩｎＰ基板がＳｉ基板よりも数倍高価であること、また半導体デバイス形成のプロセスがＳｉ基板の場合よりも複雑であるため、歩留まりが悪く、高密度に集積化できないなどの課題がある。またＩｎＰ基板はＳｉ基板よりも熱伝導が数倍悪いため、使用電力量の多い回路の集積化には適さないなどの課題があった。

【０００４】本発明は、従来のこのような課題を考慮し、光素子及び電子素子を高密度に集積化でき、低コストで歩留まりがよく、良好な特性が得られるハイブリッド集積回路とその製造方法を提供することを目的とするものである。

【０００５】

【課題を解決するための手段】請求項１の本発明は、ＩｎＰ基板と、そのＩｎＰ基板の所定の部位に形成された酸化珪素膜または珪素膜によって、ＩｎＰ基板に接合されているＳｉ基板とを備えたハイブリッド集積回路である。

【０００６】請求項６の本発明は、Ｓｉ基板およびＩｎＰ基板のそれぞれに、接合強化のための所定温度以上の温度で処理すべき半導体プロセス処理を行った後、ＩｎＰ基板に、酸化珪素膜または珪素膜を形成し、ＩｎＰ基板上に形成された酸化珪素膜または珪素膜の面を、Ｓｉ基板の所定部位に接合させ、その部位の接合力を強化す

るために所定温度で熱処理を行った後、所定温度以下の温度により、ＩｎＰ基板及びＳｉ基板上に、所定温度を下回る温度で処理すべき半導体プロセス処理を行うことによって集積化したハイブリッド集積回路の製造方法である。

【０００７】

【作用】請求項１の本発明は、ＩｎＰ基板に形成された酸化珪素膜または珪素膜が、Ｓｉ基板に接合されて、ＩｎＰ基板及びＳｉ基板が一体化された集積回路を形成する。

【０００８】請求項６の本発明は、ＩｎＰ基板上に形成された酸化珪素膜または珪素膜の面を、Ｓｉ基板の所定部位に接合させ、その部位の接合力を強化するために所定温度で熱処理を行っているので、ＩｎＰ基板とＳｉ基板とを、容易に十分な強度の接合力で接合することができる。

【０００９】

【実施例】以下、本発明にかかる実施例のハイブリッド集積回路及びその製造方法について、図面を参照しながら説明する。

【００１０】（実施例１）図１は、本発明の第１の実施例のハイブリッド集積回路の構造を示す模式断面図である。すなわち、ハイブリッド集積回路を構成しているＳｉ基板１上には、トランジスタなどの電子素子５が形成され、ＩｎＰ基板２上には、半導体レーザなどの光素子４が形成されている。又ＩｎＰ基板２の所定の面には、酸化珪素膜（または珪素膜）３が形成され、その酸化珪素膜（又は珪素膜）３とＳｉ基板１とは直接接合されている（接合の方法については後述）。それぞれの基板に形成された光素子４及び電子素子５は、電気的配線等により機能的に接続されている。

【００１１】以上のように、光素子４は、発光などの光特性に優れたＩｎＰ基板２上に形成されており、トランジスタなどの電子素子５は、大規模集積回路の形成に適したＳｉ基板１上に形成されているので、高性能の光素子４と大規模集積化した電子素子５を一体にして集積化することが可能であった。またＳｉ基板１は、熱伝導率が大きいため、ＩｎＰ基板２に高出力の半導体レーザーを形成しても、十分放熱することが可能であり、したがって、また電力増幅器などの電子素子を集積化することもできた。

【００１２】（実施例２）図２は、本発明の第２の実施例のハイブリッド集積回路の構造を示す模式断面図である。すなわち、ハイブリッド集積回路を構成しているＳｉ基板１上には、トランジスタなどの電子素子５が形成され、ＩｎＰ基板２のＳｉ基板１に対向する面の一部には、例えば半導体レーザなどの光素子（発光素子）４が形成されている。又その面の光素子（発光素子）４の周囲の所定の部位には、酸化珪素膜（又は珪素膜）３が形成され、その酸化珪素膜（又は珪素膜）３とＳｉ基板１

とは直接接合されている（接合の方法については後述）。更にＩｎＰ基板２に形成された光素子（発光素子）４に対向するＳｉ基板１の部位には、ホトダイオードなどの光素子（受光素子）４’が形成され、それら光素子（発光素子）４と光素子（受光素子）４’は光で結合されるようになっている。それぞれの基板に形成された光素子４，４’と電子素子５は、必要に応じ電気的配線及び前述の光的結合により機能的に接続されている。

【００１３】以上のように、半導体レーザなどの光素子４は、発光などの光特性に優れたＩｎＰ基板２上に形成されており、ホトダイオードなどのようにＳｉ基板１上でも高性能の得られる一部の光素子４’や、トランジスタなどの電子素子５は、大規模集積回路の形成に適したＳｉ基板１上に形成されているので、高性能の光素子４，４’と大規模集積化した電子素子５を集積化することが可能であった。これにより実施例１と同様の効果が得られた。またこの場合には、前述したようにＳｉ基板１上の大規模集積回路とＩｎＰ基板２上の光素子４を、電気的配線によらずに、光で信号を直接伝送することも可能であった。またＩｎＰ基板２上に、高速の電子素子を同時に集積化することも可能であった。

【００１４】なお、上記いずれの実施例においても、ＩｎＰ基板に形成される酸化珪素膜に代えて、非晶質の珪素膜あるいは多結晶の珪素膜を用いてもよい。

【００１５】また、上記実施例では、ＩｎＰ基板側に発光素子を形成し、Ｓｉ基板側に受光素子を形成して両基板を光により結合したが、これとは逆にＩｎＰ基板側に受光素子を形成し、Ｓｉ基板側に発光素子を形成して光による結合を行ってもよい。

【００１６】また、上記実施例では、発光素子及び受光素子の間は空間であったが、これに限らず、発光素子から発射される光が受光素子に入射されるように構成されていればよい。

【００１７】（実施例３）本発明の第３の実施例のハイブリッド集積回路の製造方法について説明する。

【００１８】まず、Ｓｉ基板およびＩｎＰ基板の所定の箇所に、接合力強化のために必要な熱処理温度以上の温度で行うべきプロセス、例えば、拡散プロセスなどを含めて、一連の半導体プロセス処理を行い、電界効果トランジスタ（ＦＥＴ）などの電子素子や半導体レーザーなどの光素子を形成した。それら拡散プロセスなどは、通常１０００度Ｃ以上の高温で行われる。

【００１９】次に、各種素子が形成されたＳｉ部およびＩｎＰ部に保護膜を形成した後、その他の露出Ｓｉ部およびＩｎＰ部の表面を極めて清浄にした。具体的には、ＩｎＰ基板は、過酸化水素とアンモニア系エッチング液で表面層をエッチング除去した。同じくＳｉ基板表面は弗酸系エッチング液により清浄化した。その時必要部分のみ保護膜を除去した。その後、ＩｎＰ基板上に化学気相成長法などにより酸化珪素膜を形成した。膜厚は０．

5

1－3ミクロン程度であり、この厚み及びその厚みの均一性の制御は容易である。さらに酸化珪素膜表面は、バッファード弗酸により清浄化した。その時必要部分のみ保護膜を除去した。

【0020】その後、酸化珪素膜の表面を純水で十分洗浄し、前記Si基板露出部に前記InP基板の酸化珪素膜を一様に重ねあわせると、酸化珪素膜表面およびSi基板表面に吸着した水酸基によって、容易に直接接合が得られた。このままでも十分な接合強度が得られるが、さらにこの状態で、100度Cから700度Cの温度で熱処理を行うと、その接合は更に強化された。ここで熱処理温度が高い場合、InP基板の熱膨張率及びSi基板の熱膨張率に差があるため、形状、寸法などに多少の制約が加えられるが、基本的には、高温で熱処理する場合ほど、接合する基板の厚みを薄く、また面積を小さくしていけば、剥離や破損なく接合強度の向上が可能であった。

【0021】次に、接合力強化のための熱処理温度以下の温度で処理すべき各種プロセス、例えば電極形成などを実施し、配線パターンを形成した。配線にはアミニウムや金などを用いた。これにより、実施例2に示す構造のハイブリッド集積回路が得られた。接合強化の熱処理効果は、例えば、200度Cで、1時間程度保持するだけでも接合強度は数倍に上がり、数10Kg／平方cmの強度が得られた。700度C以上に温度を上げると、InP基板表面からP（りん）が抜けていくため表面の特性劣化が大きく光素子としての所定の性能が得られないので、接合熱処理温度は700度C以下とすることが望ましい。

【0022】上述のSi基板1と酸化珪素膜（又は珪素膜）3との接合を、一般の樹脂などの接着剤を用いて行うと、耐熱性や耐薬品性の面から、接合後は半導体プロセスが行えないなどの問題点があるが、本実施例の方法を用いれば、Si基板とInP基板が直接接合されており、そのような問題点が解決された。

【0023】また樹脂などの接着剤を用いて接着すると、接着剤の厚みを高精度で制御することが困難なため、接着後の基板平行度が悪くなり、ホトリソグラフィーの精度が悪くなるが、そのような問題も解決された。また直接接合の場合の方が、熱伝導がよくなるため、消費電力の大きい回路にも適用することができた。

【0024】以上の直接接合のメカニズムは、珪素膜または酸化珪素膜表面を、適当な表面処理を行った後純水に浸すことにより、その表面に水酸基が付着し、接合させようとする両表面に付着した水酸基によって、接合が行われると考えられる。その後熱処理を行うと、相互拡散により接合が強化されるものと考えられる。

【0025】（実施例4）本発明の第4の実施例のハイブリッド集積回路の製造方法について説明する。

【0026】実施例3と同様にして、Si基板およびInP基板の所定の箇所に、電子素子または光素子を形成し、その後、保護膜形成、表面洗浄を行った後、接合面になるInP基板上に、非晶質珪素の膜を、プラズマCVDなどにより形成した。形成する非晶質珪素の膜厚は、実施例3の場合とほぼ同様、0．1－3ミクロン程度である。その後、実施例3と同様に、非晶質珪素膜とSi基板表面を極めて清浄にした。具体的方法は、実施例3とほぼ同じである。非晶質珪素膜表面は、バッファード弗酸系エッチング液により清浄化した。その後非晶質珪素膜及びSi基板の表面を純水で十分洗浄し、すぐに一様に重ねあわせることにより、非晶質珪素膜表面に吸着した水酸基により、容易に接合が得られた。

【0027】次に必要に応じて実施例3と同様のプロセスを行うことにより、InP基板上に形成された光素子と、Si基板上に形成された電子素子が一体に集積化されたハイブリッド集積回路の製造が可能となり、実施例3と同様の効果が得られた。この場合の接合強度は、酸化珪素膜を用いた場合よりも、2－5倍の値が得られた。

【0028】（実施例5）本発明の第5の実施例のハイブリッド集積回路の製造方法について説明する。

【0029】実施例3または4と同様にして、Si基板およびInP基板の所定の箇所に、電子素子または光素子を形成し、その後、保護膜形成、表面洗浄を行った後、接合面になるInP基板上に、酸化珪素膜または非晶質珪素膜を形成した。その後、実施例3または4と同様に、酸化珪素膜または非晶質珪素膜とSi基板表面を極めて清浄にした。具体的方法は、実施例3または4とほぼ同じである。酸化珪素膜または非晶質珪素膜表面は、バッファード弗酸系エッチング液により清浄化した。その後酸化珪素膜又は非晶質珪素膜の表面を純水で十分洗浄し、接合させる面を重ね合わた。

【0030】乾燥後、両基板を加熱しながら、酸化珪素膜部または非晶質珪素膜部に高電圧の直流電圧を加えた。これにより静電力が働き、強固な直接接合が得られた。次に必要に応じて実施例3と同様のプロセスを行うことにより、InP基板上に形成された光素子と、とSi基板上に形成された電子素子が一体に集積化されたハイブリッド集積回路の製造が可能となり、実施例3と同様の効果が得られた。この場合の接合強度は、単に熱処理したものよりもさらに強くなった。

【0031】このとき、接合部の膜に高電圧が加わるように、Si基板およびInP基板に半導体性基板を用いたり、基板一部に低抵抗部を設けることにより、接合に用いる酸化珪素膜または非晶質珪素膜に有効に高電圧を加えることができた。この場合酸化珪素膜は本来、高抵抗であるが、非晶質珪素膜の場合は、できるだけ高抵抗にすることが望ましい。

【0032】印加する電圧は、1ミクロンの膜厚に対し、50から1000Vが適当であり、電圧が高い場合

は、パルス的に加える方が良かった。

【００３３】（実施例６）本発明の第６の実施例のハイブリッド集積回路の製造方法について説明する。

【００３４】実施例３と同様にして、Ｓｉ基板およびＩｎＰ基板の所定の箇所に、電子素子または光素子を形成し、その後、保護膜形成、表面洗浄を行った後、接合面になるＩｎＰ基板上に、多結晶珪素の膜を、プラズマＣＶＤなどにより形成した。形成する多結晶珪素の膜厚は、実施例３の場合とほぼ同様、０．１－３ミクロン程度である。その後、実施例３と同様に、多結晶珪素膜とＳｉ基板表面を極めて清浄にした。具体的方法は、実施例３とほぼ同じである。多結晶珪素膜表面は、バッファード弗酸系エッチング液により清浄化した。その後多結晶珪素膜及びＳｉ基板の表面を純水で十分洗浄し、すぐに一様に重ねあわせることにより、多結晶珪素膜表面に吸着した水酸基により、容易に接合が得られた。次に必要に応じて実施例３と同様のプロセスを行うことにより、ＩｎＰ基板上に形成された光素子と、Ｓｉ基板上に形成された電子素子が一体に集積化されたハイブリッド集積回路の製造が可能となり、実施例３と同様の効果が得られた。

【００３５】なお、上記ハイブリッド集積回路の製造方法の実施例では、いずれも、実施例２の構造の例について説明したが、実施例１の構造を得るには、各製造方法の実施例において、酸化珪素膜または珪素膜を、単にＩｎＰ基板の裏面に形成すれば実現することができた。この場合のＩｎＰ基板上の光素子などと、Ｓｉ基板上の電子素子などとの結線は、外部のワイヤーで行ったり、ＩｎＰ基板にビアホールを形成するなどして行った。

【００３６】また、上記実施例では、いずれも、Ｓｉ基板上には他の膜を形成しなかったが、Ｓｉ基板上にも酸化珪素膜又は珪素膜を形成しても同様の直接接合が可能であった。

【００３７】また、上記実施例では、いずれの場合も接合に用いる膜表面の平坦度が重要であり、製膜の方法、

条件が悪く、表面の凹凸が大きい場合には接合が困難となるため、十分な注意が必要であった。

【００３８】また、いずれの実施例においても、まず第１に、Ｓｉ基板に形成された電子素子などとＩｎＰ基板に形成された光素子などを、一体に集積しているので、ハイブリッド集積回路を大幅に小型、軽量化する事が可能となった。

【００３９】また、大規模集積回路は、歩留まり良く形成できるＳｉ基板上に、光素子は高性能の得られるＩｎＰ基板上に形成できるため、単一基板を用いて集積した場合よりも、高性能のハイブリッド集積回路が歩留まり良く得られた。

【００４０】また、いずれの実施例においても、接合方法は、ＩｎＰ基板とＳｉ基板を膜厚の制御された珪素系無機材料で直接接合しているので、平面性が極めて良く、大規模集積に必要な、サブミクロンのホトリソグラフィーが可能となるとともに、熱や振動などに対する信頼性も大幅に向上した。

【００４１】

【発明の効果】以上述べたところから明らかなように本発明は、光素子及び電子素子を高密度に集積化でき、低コストで歩留まりがよく、良好な特性が得られるという長所がある。

【図面の簡単な説明】

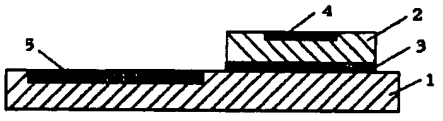
【図１】本発明にかかる第１の実施例のハイブリッド集積回路の構成を示す模式断面図である。

【図２】本発明にかかる第２の実施例のハイブリッド集積回路の構成を示す模式断面図である。

【符号の説明】

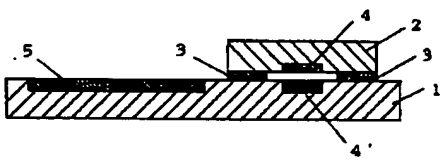
1	Ｓｉ基板
2	ＩｎＰ基板
3	酸化珪素膜または珪素膜
4	光素子（発光素子）
4'	光素子（受光素子）
5	電子素子

【図１】



1　Ｓｉ基板
2　ＩｎＰ基板
3　酸化珪素膜または珪素膜
4、4'　光素子
5　電子素子

【図２】



フロントページの続き

(72)発明者　小掠　哲義
大阪府門真市大字門真1006番地　松下電器
産業株式会社内